National Advanced Systems

AS/9000 Series

Product description

PREFACE

This Product Description introduces the hardware, microcode, and the basic operating and functional characteristics of the National Advanced Systems AS/9000 series of IBM compatible processor complexes. It is assumed that the reader will have some familiarity with IBM System/370 processors.

| This is the fourth edition of this manual. | It has had a number of corrections made to | the descriptions of the AS/9000 series.
|
| The third edition of this manual was | completely rewritten to reflect the | introduction of the AS/9040, AS/9050, | AS/9060, AS/9070 and AS/9080 processors to | the Advanced System 9000 Series. An | appendix has been included to describe the | various changes which have been made to the | specifications of the AS/9000 processors. This upgrading of specifications has made some of the features which were originally optional on the processors standard.

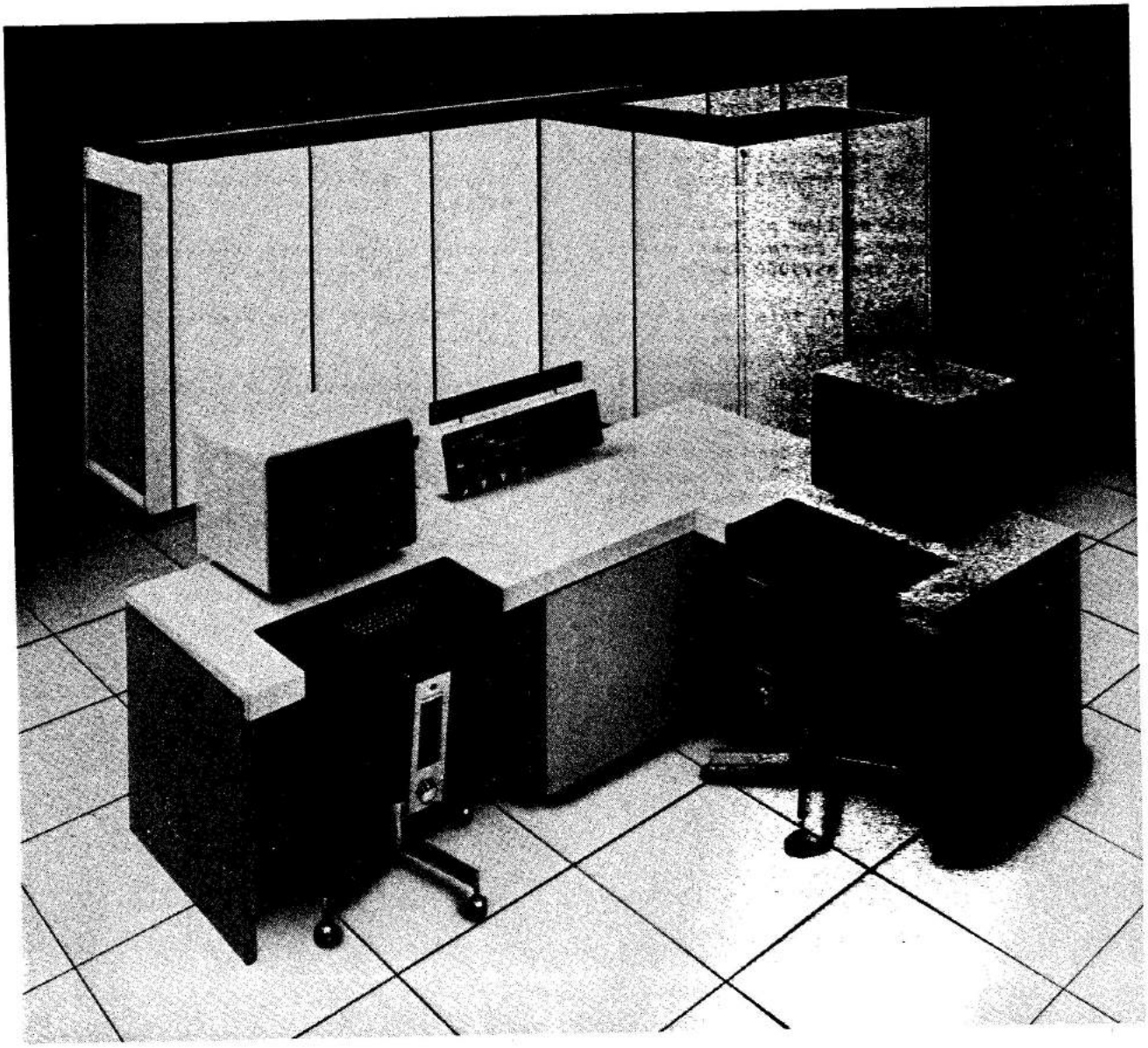
Other reference material relative to the AS/9000 series processors is available.

This includes the following from National Advanced Systems:-

- Advanced System 9000 Series Functional Characteristics.
- Advanced System 9000 Series Operators Guide.

| The following additional reference material | from IBM is also available:-

- IBM System/370 Principles of Operation. (GA22-7000)
- Virtual Machine Assist and Shadow Table Bypass Assist. (GA22-7074)
- IBM System/370 Assists for MVS. (GA22-7079)
- IBM System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturers' Information. (GA22-6974)



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AS/9000 SERIES INTRODUCTION

PRODUCT OVERVIEW

The Advanced System 9000 comprises a family of large scale IBM compatible processors designed to be the most powerful and reliable general purpose computers available in the marketplace. Through modular construction in conjunction with the extensive use of microcode in the CPU, Service Processor and I/O Processors the AS/9000 series of processors provide total compatibility with the comparable large scale IBM processors.

The AS/9000 family of processors includes the following:-

- The AS/9040 (Uni-Processor).
- The AS/9050 (Uni-processor).
- The AS/9060 (Uni-Processor).
- The AS/9070 (Dual Processor Complex).
- The AS/9080 (Dual Processor Complex).

The AS/9000 Series processors support IBM's MVS and VM/370 operating systems without the requirement for hardware or software modifications. The uni-processor models will also support the VS/1 operating system.

HIGHLIGHTS

- Full functional IBM compatibility.
- MVS and VM assists are available.
- Completely air-cooled.
- Modular hardware design and extensive use of microcode permits NAS to follow any future enhancements to the IBM architecture.
- Designed to have the highest possible reliability.

AS/9000 SERIES PERFORMANCE

As new releases of operating systems supporting new architecture and/or functions become available, the absolute rate at which instructions are executed within any processor may well change. It is possible, and in fact highly likely, that the rate of instruction execution will decrease even though the overall throughput of the system will increase. In most cases the relative instruction execution rate ratios between AS/9000 Series processors should however remain constant where similar workloads are run in similar configurations.

Since measuring the performance of a system based on throughput is highly dependent on the configuration, applications, and operating characteristics, specific workloads should be carefully evaluated before projecting an estimate of throughput based on the instruction execution rates of the processors. The AS/9050 basic model has an internal instruction processing speed generally in the range of 8 to 10 million instructions per second (MIPS). This gives a performance relative to the NAS AS/7000 processor of between 2.4 and 2.6 times. The lower end of the range will be seen in environments such as dedicated use of MVS/IMS and the higher end in environments such as commercial or scientific batch work.

Table 1 on page 2 shows the relative performance of the AS/9000 series of processors.

CPU Model	AS/7000	AS/9040	AS/9050	AS/9060	AS/9070	AS/9080
AS/7000	1	2.03-2.50	2.53-3.13	3.33-4.00	4.50-5.70	6.00-7.20
AS/9040	0.41-0.47	1	1.12-1.38	1.47-1.76	1.99-2.51	2.65-3.18
AS/9050	0.33-0.38	0.72-0.88	1	1.18-1.41	1.70-1.90	2.12-2.54
AS/9060	0.25-0.29	0.55-0.69	0.69-0.85	1	1.23-1.55	1.70-1.80
AS/9070	0.18-0.21	0.40-0.49	0.50-0.61	0.65-0.78	1	1.18-1.41
AS/9080	0.14-0.16	0.31-0.38	0.38-0.47	0.51-0.61	0.68-0.86	1

Table 1 - Relative AS/9000 Series Performance.

AS/9000 ARCHITECTURE

TECHNOLOGY

The AS/9000 family utilises a mixture of highly reliable Emitter Coupled Logic (ECL) intergrated circuit types. This results in a processor which gives the user the maximum possible availability.

In addition special types of intergrated circuit such as the 'Logic in Memory' LSI are used in areas such as cache buffer addressing and the Translate Lookaside Buffer (TLB) where extremely high speed processing of small amounts of data is required. These components complement the very fast internal processing speeds of the AS/9000 series of processors. Table 2 gives a summary of the major characteristics of the hardware logic used in the AS/9000 Series of processors.

VLSI	Max. number of gates	1500
	Gate delay (ns)	0.45
	Number of pins	108
	Average Power (W)	3.3
LSI	Max. number of gates	550
	Gate delay (ns)	0.35
	Number of pins	108
	Average Power (W)	3.3
MSI/SSI	Number of gates	70-3
	Gate delay (ns)	0.75
	Number of pins	24
	Average Power (W)	0.8-0.1
Logic in memory LSI	Capacity (kilobits)	6 & 3
	No. of gates	770 & 470
High speed bipolar RAM	Capacity (kilobits)	1 or 4
	Chip Access (ns)	7
NMOS memory chip	Size (kilobits)	64 or 16
	Chip Access (ns)	100
Pluggable board (packages)	No. of layers	10
	Grid pitch (mm)	1.91
Backboard (platters)	No. of layers	14 & 18
	Grid pitch (mm)	2.54

** ns=nanoseconds W=watts mm=millimeters

Table 2 - Hardware Components of the AS/9000.

The high speed bipolar RAM is used in the high speed buffer (cache memory) and can be accessed in half of the processors basic cycle time. This RAM is also used for the Processor Control Storage which holds the microcode used to drive the AS/9000 system.

The AS/9000 series of processors are completely air-cooled and are supplied as standard with their own power distribution motor generator units.

AS/9000 SERIES SYSTEM UNITS

An AS/9000 processor complex will contain:-

- One or two Basic Processor Units (BPU's).
- A minimum of one input/output processor frame per BPU.
- A minimum of one Service Processor (SVP) per BPU, each with two four colour displays with full function keyboards.
- Between two and five Power Distribution Units (PDU's), depending on the exact configuration.
- One main memory frame.

Table 3 on page 5 shows which main units will comprise each model of the AS/9000 processor complex.

Figure 1 on page 4 shows the logical layout of the functional units of an AS/9000 processor. The exact combination of units in any specific AS/9000 processor complex will depend on the model and the optional features which are installed. In particular the exact number of PDU's is very dependent on the combination of features installed and a detailed analysis will be needed to work out when an additional PDU will be required.

BASIC PROCESSOR UNIT (BPU)

Although detail differences exist within the

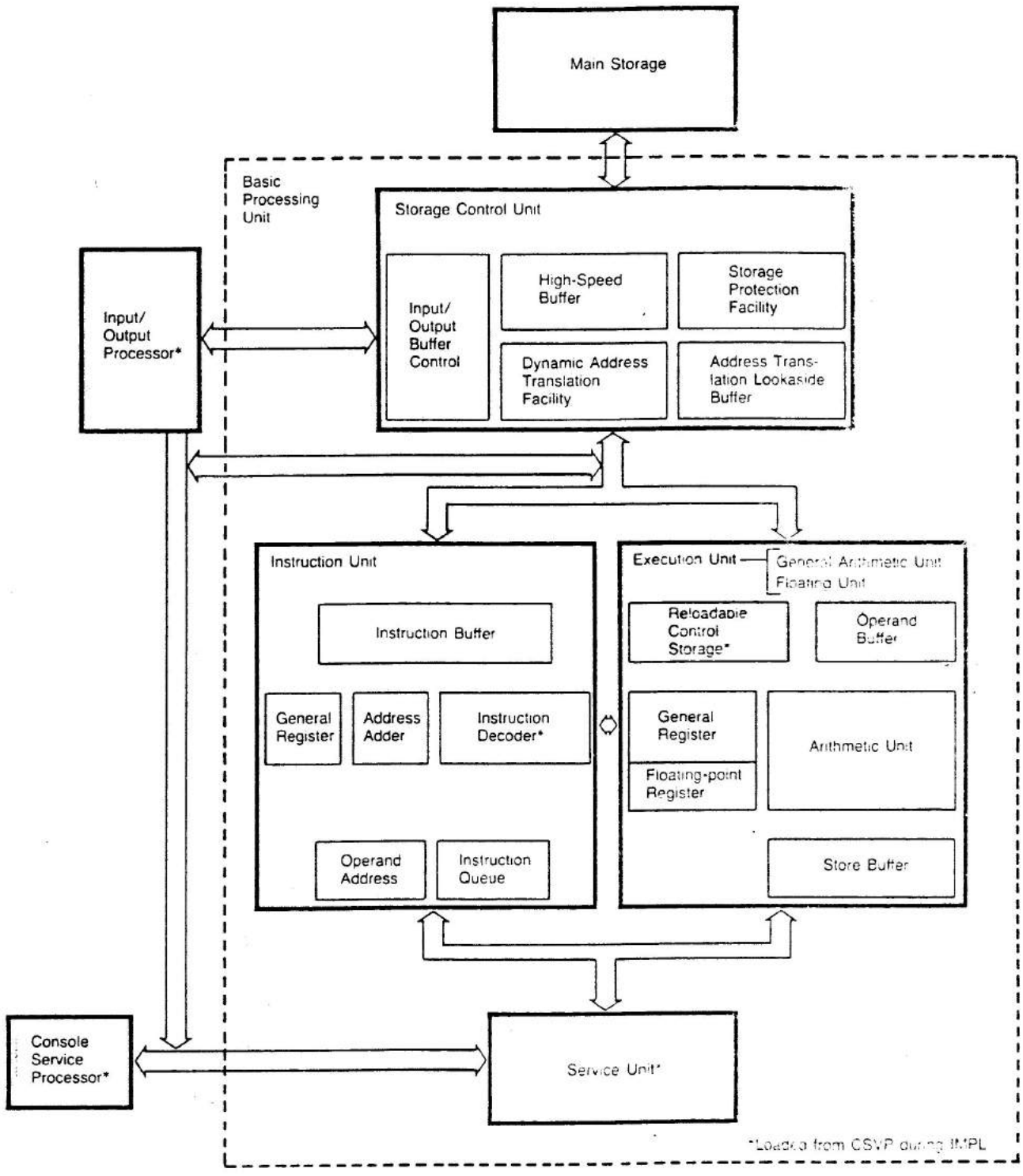

Figure 1 - AS/9000 Functional Layout.

AS/9000 Series Model	BPU's	IOP's §1	SVP's	PDU's	Main Memory Frame
AS/9040					
Basic 8 chans/8 Mbytes	1	1	1	2	1
Max 16 chans/24 Mbytes	1	2	1	2	1
AS/9050					
Basic 16 chans/16 Mbytes	1	2	1	2	1
Max 24 chans/32 Mbytes	1	3	1	3	1
AS/9060					
Basic 16 chans/16 Mbytes	1	2	1	2	1
Max 24 chans/32 Mbytes	1	3	1	3	1
AS/9070					
Basic 16 chans/16 Mbytes	2	2	2	5	1
Max 32 chans/32 Mbytes	2	4	2	5	1
AS/9080					
Basic 16 chans/16 Mbytes	2	2	2	5	1
Max 32 chans/64 Mbytes	2	4	2	5	1

§1 An additional physical frame is only required when more than two IOP's are installed on uniprocessor models.

Table 3 - Basic AS/9000 Processor Configurations.

BPU's used for the different models in the AS/9000 Series the basic design and layout is essentially the same.
Each BPU contains:-

- An Instruction Unit (IU).
- An Execution Unit (EU).
- A High Speed Arithmetic Unit (HSA).

Following is a more detailed description of each individual unit.

THE INSTRUCTION UNIT (IU)

This unit fetches program instructions from memory into a 'pipeline' and prepares them for execution by the Execution Unit (EU). Branches whose outcome cannot be accurately predicted by the IU Branch Prediction Logic result in the creation of an 'alternate pipeline'. Into this new 'pipeline' are placed instructions from the alternate branch path which are fetched and decoded until such time as the outcome of the branch instruction is resolved. The IU also prefetches instruction operands and does some of the validity checking of the operand data. Much of the IU processing is done under the control of data loaded into the IU memory which helps to make the introduction of new instructions or functions to the AS/9000 series very easy.

The ability of the IU to work in parallel with other parts of the processor complex saves the EU from many delays and is in part responsible for the very high processing speeds of the AS/9000 series of processors.

THE EXECUTION UNIT (EU)

This part of the BPU is responsible for the execution of the arithmetic and logical operations specified by the instructions which have been set up for it by the IU. The EU contains the following:-

- A local high speed storage containing:-
  - the 16 four-byte general purpose registers (GPR's).
  - the 4 eight-byte floating point registers (FPR's).
  - a number of internal work registers used by the EU whilst executing the instructions.

- The 'control storage' which holds the microprograms and data used to control the processor hardware.
- An Arithmetic/Logic Unit (ALU) each of whose sub-units can operate concurrently under the control of the EU microcode. The sub-units contained in the ALU are:-
  - a parallel adder unit.
  - a shifter unit.
  - a serial adder unit.
- A High Speed Arithmetic unit (HSA), which is designed to carry out selected arithmetic instructions faster than the normal ALU.
  The HSA is controlled by it's own microcode and executes one microword in half the basic cycle time of the processor to which it is attached. The HSA unit increases the speed of the processor for the execution of all floating-point multiply and divide instructions and also for most of the fixed-point multiply instructions.

When executing an instruction from the processors instruction set, the EU starts off with information pre-processed for it by the IU. The IU places information (operands) into some of the EU's work registers, then references the starting micro-instruction in the control storage which is contained within the EU. Since many instructions only require one microword to execute them the starting micro-instruction may also be the only one to be executed.

The basic unit of operation in the EU is the gating of one or more registers through the serial adder, parallel adder or the shifter to another register. This gating takes place within one machine cycle and is controlled by the execution of a single micro-instruction. Simple instructions, requiring only one such operation for execution, are thus completed in one machine cycle.

More complex instructions have to be controlled by a series of micro-instructions executed one after the other. Each micro-instruction contains within itself sufficient information to specify the address of the next micro-instruction to be executed. The last micro-instruction in any such sequence contains an indication, the End of Processing bit (EOP), that it is the last micro-instruction needed for the execution of the instruction.

The EOP bit, when set to one, causes the next starting micro-instruction address to be loaded from the active IU which causes execution to begin on the next instruction in the IU pipeline.

INPUT OUTPUT PROCESSOR (IOP)

The IOP is responsible for the transfer of data between the processor main storage and various peripheral devices attached to the IOP's channels. The AS/9000 series IOP supports up to eight channels by use of it's own microprogram controlled processor. Each channel within the IOP is also run under microprogram control. Separate Reloadable Control Stores are provided within the IOP for each channel as well as for the IOP's controlling functions. Each IOP runs independently and in parallel with the operations in other IOP's and/or BPU's in the processor complex.

Additional logic is provided in all the independent functions in an AS/9000 processor complex to resolve any priority or interlocking requirements which might arise from the parallel processing. For example when the IOP stores data into main memory it would be possible for the BPU units to already be using the same storage area via the high speed cache memory.

To ensure that the BPU cache is always valid, storing of data by the IOP causes any block of data in the cache which is at the same address to be marked 'cancelled'. This operation of 'block cancel' forces the BPU to refetch any data changed by the IOP and thus maintains the overall integrity of the system.

The channels on the AS/9000 IOP are fully compatible with the equivalent IBM System/370 channels and will support all peripheral devices which conform to the IBM specifications. (See IBM manual GA22-6974 for specifications of the interface.)

Each IOP provides 8 I/O channels for the attachment of peripherals to the processor complex. Each channel is provided with 256 Unit Control Words (UCW's). UCW attributes, channel type and channel number assignments are all set up by entering the relevant information into the IOP from the SVP and require no engineering activity to alter them.

Each channel can be set up to be any one of the following types:-

- Byte Multiplex. (A maximum of two within any one IOP)
- Low speed Block Multiplex. (Standard and Offset Interlock)
- High speed Block Multiplex. (Data Streaming Mode)

SERVICE PROCESSOR (SVP)

The SVP is used to provide the operational control and maintenance facilities for the entire processor complex. The SVP is designed to be attached to the various components of the processor complex via it's own specially designed interfaces. When the SVP is used in conjunction with the console display the combination is normally referred to as the Console Service Processor (CSVP). Each SVP is divided into two independent operator stations each of which contain the following components:-

o An independent micro-program controlled processor that supports some 25 different functional frames.

o A full function 'QWERTY' (§1) keyboard that also includes:-
  - 12 program function keys.
  - PA1 key.
  - Insert, delete, copy, erase EOF (End Of File), enter, clear and cancel keys.
  - up, down, left and right keys to control cursor movement.
  - start, stop and external interrupt keys to control the processor.
  - select frame key to control the functional frame to be used.
  - a request key for use when the console is running in 'printer/keyboard' mode.

o One 20 inch four colour CRT display.

o A standard IBM System/370 interface, complete with two channel switch, which is used to connect the operator station with the I/O channels of the AS/9000 processor complex.

o A read/write diskette drive ('floppy disk') used to contain:-
  - operational microcode for the various parts of the processor complex.
  - various diagnostic programs used to test the processor complex.
  - logout files which are used to record the the system environment at the time at which a failure has been detected.
  - programs which are used to analyse any failures which may have been recorded as logout files.

Both of the display stations in the SVP can be used concurrently as consoles under the control of the operating system. When required however either of the display stations may be used to provide the service support functions.

The AS/9000 provides operational redundancy within the SVP by duplicating all of the components in the operator stations except the power supplies. In addition either operator station has the ability to carry out all the functions of the other operator station.

CONSOLE FUNCTIONS

The CSVP is used to perform the following major functions for the AS/9000 processor complex:-

o Initiate 'Power On' and 'Power Off' sequences.

o Initialise all the components of an AS/9000 complex, and verify that the system components have initialised correctly.

o To save certain data about a specific configuration (e.g. Unit Control Word information.) and ensure that the complex is always initialised with the appropriate information.

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§1 QWERTY is used as an abbreviation for a standard English language typewriter keyboard. It refers to the starting sequence of alpha keys on the second row of the keyboard.

- Control the operations of the processor complex (start, stop, etc.) and whilst functioning as a console communicate with the system control program being used.

- Control the diagnostic and maintenance facilities used to resolve any system malfunctions which might occur.

A control panel on the AS/9000 SVP provides basic power on/off, SVP initial Micro Program Load (IMPL), I/O interface enable/disable, Time of Day (TOD) clock set enable and audible alarm controls. A panel of lamps is provided on the SVP to indicate the basic operating status of the processor complex.

MAIN MEMORY

Main Memory utilises 64K NMOS chips to provide main storage for the AS/9000 processor complex. Depending on Model and features installed up to 64 Megabytes of storage can be provided. Main storage uses Error Correction Circuits (ECC) to provide automatic recovery from 'single-bit' storage errors and detection of multi-bit errors. Use is made of 8-way interleave on UP models and 16-way on DPC models to increase aggregate memory data-transfer rates. Figure 2 on page 9 shows how main storage is configured.

Each memory is structured from logical 2 Mbyte modules up to the maximum of 32 Mbytes. Each module can be thought of as being stacked up vertically in 2 Mbyte increments. The starting address assigned to each module is set up from the SVP. All modules are divided up into 8 parallel 256K byte banks each of which have a data width of 8 bytes. The SCU accesses memory by interleaving memory requests in 8 byte multiples.

Data is transferred from main memory to the high speed buffer in units of 64 bytes. This is achieved by requesting that two immediately consecutive 32 byte blocks of data are to be transferred from main memory.

When the system configuration includes two BPU's the memory layout described above is duplicated in parallel. This results in the memory becoming 16 way interleaved instead of the single processor 8 way and the maximum memory size being increased to 64 M/bytes.

FEATURES

All AS/9000 processor complexes include as standard a number of features which are optional on IBM System/370 systems. Table 4 on page 10 gives a list of these features.

Most of the features require that some specific level of IBM SCP be used to control the system to permit their use. It is more common therefore to apply some 'generic' names to cover more than one specific feature. This convention has been followed when describing the features which are standard or optional for the AS/9000 series of processors. In addition in some cases, for example Dual Address Space, changes are required to the hardware definitions, microcode and the SCP for the feature to become usable.

The following list identifies the generic feature names used to describe IBM compatible features available for the AS/9000 series of processors:-

- System/370 Extended Facility (S/370 EF).

- Virtual Machine Assist (VMA).

- MVS/SP Assists.

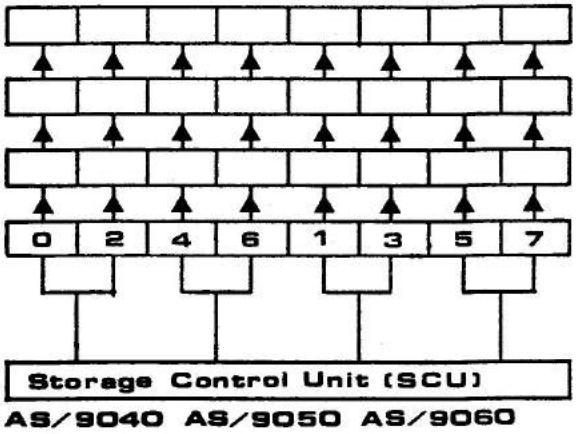
- Extended Architecture.

- PLPA Segment Protection.

- Preferred Machine Assist.

Table 5 on page 11 gives a full list of standard and optional features of the AS/9000 processor complexes.

Optional features can all be field installed when required to expand the capabilities of a system.



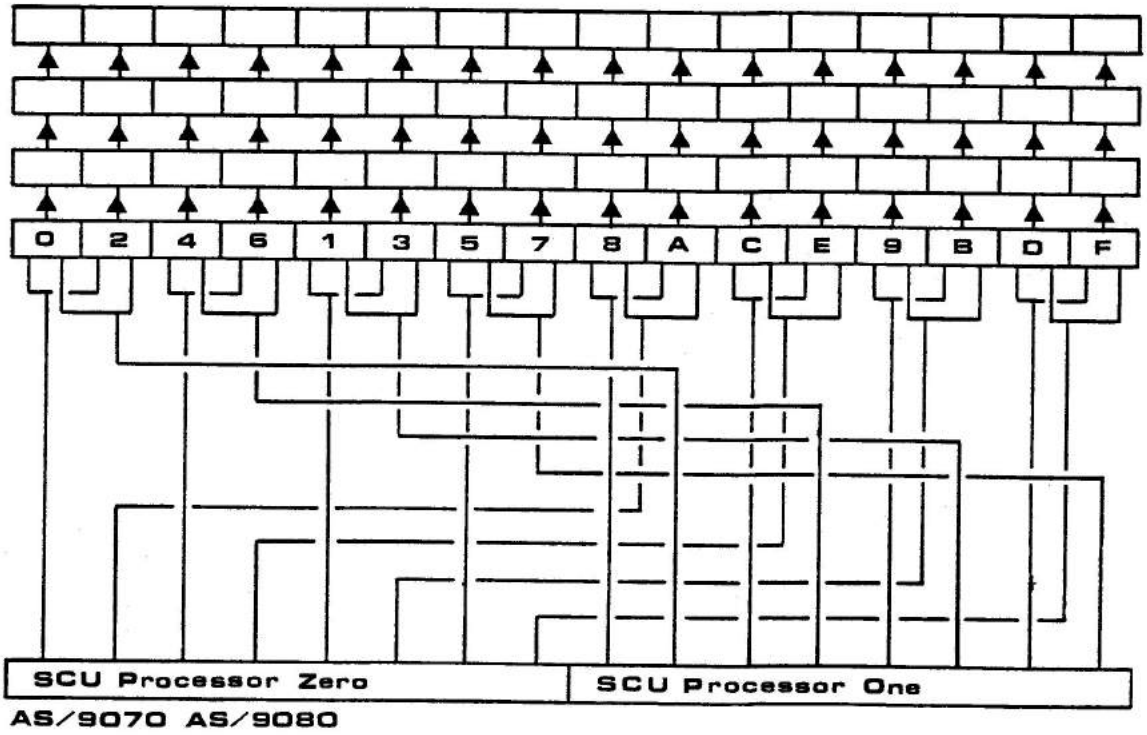


Figure 2 - Main Storage Configuration.

Facilities	9040	9050	9060	9070	9080
Commercial instruction set	S	S	S	S	S
Block-multiplexer channels	S	S	S	S	S
Branch and save	M	M	M	M	M
Byte-multiplexer channels	S	S	S	S	S
Channel indirect data addressing	S	S	S	S	S
Channel-set switching	-	-	-	S	S
Clear I/O	S	S	S	S	S
Command retry	S	S	S	S	S
Conditional swapping	S	S	S	S	S
CPU timer and clock comparator	S	S	S	S	S
Direct control	O	O	O	O	O
Dual address space	M	M	M	M	M
Extended	S	S	S	S	S
Extended-precision floating point	S	S	S	S	S
Extended real addressing	M	M	M	M	M
External signals	O	O	O	O	O
Fast release	S	S	S	S	S
Floating point	S	S	S	S	S
Halt device	S	S	S	S	S
I/O extended logout	X	X	X	X	X
Limited channel logout	X	X	X	X	X
Move inverse	S	S	S	S	S
Multiprocessing	-	-	-	S	S
PSW-key handling	M	M	M	M	M
Recovery extensions	S	S	S	S	S
Segment protection	P	P	P	P	P
Selector channels	-	-	-	-	-
Service signal	-	-	-	-	-
Start-I/O-fast queueing	M	M	M	M	M
Storage-key-instruction extensions	M	M	M	M	M
Storage-key 4K-byte blocks	M	M	M	M	M
Suspend and resume	M	M	M	M	M
Test block	M	M	M	M	M
Translation	S	S	S	S	S
31-bit IDAW's	M	M	M	M	M

- Not applicable to this AS/9000 series model.

O Optional feature on the AS/9000 series of processors.

M Known as the 'MVS/SP A †' feature for the AS/9000 series processors.

P Known as 'PLPA protection' feature for the AS/9000 series processors.

S Standard feature installed on all AS/9000 processors.

X Feature is standard but data stored is machine dependent.

(Refer to the IBM Principles of Operation for full explanation of these facilities.)

Table 4 - Standard IBM System/370 Features of the AS/9000.

Features		AS/9040	AS/9050	AS/9060	AS/9070	AS/9080
CHANNELS						
Standard		8	16	16	16	16
Increment		8	8	8	8	8
Maximum		16	24 §1	24 §1	32	32
MAIN MEMORY						
Standard		8	16	16	16	16
Increment		8	8	8	16	16
Maximum	§2	24	32	32	32	64
Interleaving		8	8	8	16	16
CTCA						
Standard		0	0	0	0	0
Max. no. of Optional CTCA's		5 §3	5 §3	5 §3	10 §4	10 §4
Extended Channel Adapter		Std	Std	Std	Std	Std
Extended Channel Groups		Std	Std	Std	Std	Std
Extended Addressing	§5	Std	Std	Std	Std	Std
Direct Control		Opt	Opt	Opt	Opt	Opt
First Printer per SVP	§6	Opt	Opt	Opt	Opt	Opt
Second Printer per SVP		Opt	Opt	Opt	Opt	Opt
Data Streaming Capability		Std	Std	Std	Std	Std
System/370 Extended Facility		Std	Std	Std	Std	Std
Virtual Machine Assist		Std	Std	Std	Std	Std
MVS/SP Assists		Std	Std	Std	Std	Std
PLPA Segment Protection	§7	Opt	Opt	Opt	Opt	Opt
Extended Architecture	§7	Opt	Opt	Opt	Opt	Opt
Preferred Machine Assist	§7	Opt	Opt	Opt	Opt	Opt
High Speed Arithmetic		Std	Std	Std	Std	Std
First SVP		Std	Std	Std	Std	Std
Second SVP		Opt	Opt	Opt	Opt	Opt

§1 Extended Architecture is a pre-requisite if more than 16 channels are to be used.

§2 Additional storage is provided in increments of 8 M/bytes for the AS/9040, AS/9050 and AS/9060 models. Additional storage is provided in increments of 16 M/bytes for the AS/9070 and AS/9080 models. Use of more than 16 M/bytes of storage requires that the MVS/SP Assist feature or the Extended Architecture feature be installed.

§3 The first optional CTCA is installed within the existing AS/9000 hardware. Additional optional CTCA,s require an additional frame to be installed. The new frame takes up to four more CTCA,s in increments of two.

§4 The first two optional CTCA's are placed in the existing AS/9000. Additional CTCA's require an additional frame for each 4 additional CTCA's. After the first 2 CTCA's are installed increments to the maximum are in increments of 2.

§5 Extended Addressing will be shipped as part of 'MVS/SP assists'.

§6 One printer per standard SVP is provided on AS/9000 processors shipped via National Advanced Systems (Europe).

§7 The final date when these features will be installed depends on when IBM makes its 'First Customer Ship'. Contact your National Advanced Systems representative for the current status.

Table 5 - AS/9000 Standard and Optional Features.

SYSTEM/370 EXTENDED FACILITY (S/370 EF)

This feature enhances the capabilities and performance of the AS/9000 series of processors when running the MVS/System Extensions (MVS/SE) or the MVS/System Product (MVS/SP) program products.

The feature includes the following:-

- 4 lock-handling instructions
- 6 tracing instructions
- SVC ASSIST
- FIX PAGE
- Low Address Protection
- INVALIDATE PAGE TABLE ENTRY instruction
- TEST PROTECTION instruction
- The 'common segment' facility
- Modified READ DIRECT and WRITE DIRECT instructions

Further details can be found in the manuals indicated in the PREFACE.

VIRTUAL MACHINE ASSIST (VMA)

This feature enhances the capabilities and performance of the AS/9000 series of processors when running the VM/370 control programs.

The feature includes the following:-

- The basic 'Virtual Machine Assist' feature
- Shadow Table Bypass Assist

Further details can be found in the manuals indicated in the PREFACE.

MVS/SP ASSISTS

This feature enhances the capabilities and performance of the AS/9000 series of processors when running the MVS/SP Version 1 Release 3 program product.

The feature includes the following:-

- Dual Address Space Feature which is used by Cross Memory Services (XMS) function of the control program.
- Suspend/Resume Facility which is used to improve the performance of the paging I/O subsystem of the control program.
- Page Fault Assist which reduces the overhead of the real storage management subsystem of the control program.
- I/O Queueing Facility which offloads some of the processor overhead associated with queueing into the IOP.
- Extended Addressing which provides support for real memory sizes greater than 16 Megabytes. (Virtual memory is still limited to 16 megabytes.)

Further details can be found in the manuals indicated in the PREFACE.

EXTENDED ARCHITECURE

This feature will permit the AS/9000 series of processors to support the MVS/SP Version 2 control program and its related program products (collectively referred to as MVS/XA) and the VM/XA Migration Aid. The following is a list of the highlights of this feature:-

- Support for 31 bit real and virtual addresses.
- Support for more than 16 I/O channels per BPU.
- Provision of a 'dynamic channel subsystem' ('outboard channels').
- Bimodal operation (concurrent use of programs which use both 24 bit and 31 bit addressing).

Full details will be provided after the release of specifications by IBM.

PLPA SEGMENT PROTECTION

This feature provides a means to protect data contained in the MVS/SP Pageable Link Pack Area (PLPA) against accidental alteration. Full details will be provided after the release of specifications by IBM. The Extended Architecture feature is a prerequisite for this feature.

MICROCODE USAGE

The main BPU contains 16K words of Reloadable Control Storage (RCS), each word of which is 160 bits in length and controls various concurrent machine functions. The IOP's, HSA, SVP's and Instruction Unit (IU) also contain their own microcode.

Standard microcode features on the AS/9000 are:-

- System/370 Extended Facility (S/370 EF).
- Virtual Machine Assist (VMA).
- 3033 Extension Feature.

Optional microcode features on the AS/9000 are:-

- Extended Architecture.
- Preferred Machine Assist.

SOFTWARE SUPPORT

The Advanced System 9000 processor complexes will support all of IBM's MVS, VS/1 and VM/370 virtual operating systems without software modifications.

This page is for editorial purposes only.

RELIABILITY AVAILABILITY SERVICEABILITY

RAS HIGHLIGHTS

A primary requirement in the design of the AS/9000 series was to make available to the customer a processor which would have extremely good 'Reliability, Availability and Serviceability' (RAS) characteristics. The main factors which contribute to the excellent RAS character of the AS/9000 series are listed below. This list is followed by a more detailed description of each of them.

- Quality control of the highest possible standard is used at all stages during the manufacture and testing of an AS/9000 series processor complex.
- Design of the processor complex such that all internal malfunctions can be detected.
- The provision of as much data as possible, should a malfunction be detected, to assist the engineer in resolving problems as quickly as possible.
- Providing the ability for the processor and channels to 'retry' operations, where this can be done without loss of integrity to the failed operation.
- Emulation of IBM SYSTEM/370 is such that when a failure is presented to the IBM operating system the system reacts as if it is driving an IBM processor.
- Providing diagnostic facilities which are designed to ensure that should a failure occur that a repair can be effected in the shortest possible time.

QUALITY CONTROL

The highest possible standards of quality control are used in all stages of the design, production and testing of AS/9000 series processors. Because the ability to apply high standards of quality control is part of the initial design, the resulting processor can achieve levels of Reliability, Availability and Serviceability which are unsurpassed by other processors in the same performance class.

All the components used in the construction of the processor are repeatedly tested throughout the manufacturing process and only those that meet the most stringent requirements are used. This rigorous testing, from individual component to complete system, is designed to eliminate any component liable to failure from the delivered system. AS/9000 processor complexes are not expected to have any major failures immediately after installation.

Any failed components are returned to the factory and the cause of the failure is analysed further. This analysis will, where it is applicable, result in changes to the product. This feeding back of information about the product is part of the design aim of using quality control procedures at all levels to ensure that the product is the best possible available.

FAILURE DETECTION

Should a malfunction be detected during system operation, it is most important that the failure be detected. This is can be seen from two points of view:-

- to avoid any incorrect processing.
- in order that a fault may be located.

All AS/9000 processor complexes have been designed with these objectives in mind. The methods used in the AS/9000 series includes:-

- parity checking. (Used in most parts of the processor logic.)
- compare checking. (Used in the Service Processor and the EU Parallel Adder.)
- Hamming code check. (Used in main storage.)
- residue checking. (Used in the HSA hardware.)
- environmental checking.
- initialisation checks.

Some of these are discussed in more detail below.

HAMMING CODES

Main storage uses a 'Hamming' (§1) code to check the validity of the contents of main storage. The Hamming code is created, and then added to the data when it is placed in main memory. When data is fetched from main memory the appended Hamming code is also fetched. This Hamming code is used to recover all storage single bit errors without impacting the end user.

The same Hamming code is also used to detect any double bit errors.

RESIDUE CHECKING

The high speed arithmetic facility use a 'residue check' method to validate its processing. 'Residue checking' is a mathematical method of verifying the correct results of an arithmetic operation. By using special hardware to carry out the residue check considerable processing time is saved since continual parity type checking is not required at each step of the arithmetic operation being carried out.

ENVIRONMENTAL CHECKING

The system is provided with means to detect that the environment in which the processor is running does not exceed specified limits. If such a condition is detected the system will 'turn itself off' rather than permit damage to occur.

INITIALISATION CHECKS

During various reset operations, such as 'power On', 'System Reset', etc., special tests of the system functions are carried out. These tests verify that the major parts of the system are able to function correctly and that normal programs may be executed.

ERROR INFORMATION

If the processor detects a failure then prior to any other activity, such as instruction retry, etc., the information about the failed status of the processor is logged out to the SVP diskette. To ensure that the engineer has the best possible chance of analysing the failure correctly all information about the status of the AS/9000 is saved for later processing.

The AS/9000 has a facility called the 'Stage Tracer' which is an extremely powerful tool for use in trouble-shooting problems in the control structure of the processor. The Stage Tracer constantly records certain key signals of the processor hardware in a 'wrap around' table which automatically halts when a malfunction is detected. The Stage Tracer data can then be analysed to find out the events which preceded the detection of the malfunction.

PROCESSOR RETRY FACILITIES

The AS/9000 supports processor 'Instruction Retry' and channel 'Command Retry' facilities. These are described in more detail below.

PROCESSOR INSTRUCTION RETRY

In the BPU most processor operations can be retried if a malfunction is detected during their execution.

Part of the BPU maintains valid 'checkpoints' of the data used for the execution of an instruction. If the integrity of the instruction being executed can be maintained then a retry of that instruction, or of a step within that instruction, will be carried out. Up to seven retries will be carried out before any malfunction is considered to be permanent.

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§1 'Hamming' codes are named after the originator of some specific algorithms commonly used to validate data fields in modern computers.

Instruction retry can allow the system to handle many intermittent errors which might otherwise have resulted in the complete loss of the processor complex to the user. The information about the failure is of course recorded on the SVP diskette, even though the system continues processing, to ensure that the engineer can analyse the intermittent failure.

CHANNEL COMMAND RETRY

Many current peripheral devices are able to request that the channel is to reissue I/O commands which may have failed. This facility supports such peripherals. I/O commands retried by this facility cause no interrupt to be presented to the processor and thus eliminate some of the overhead associated with failures in peripheral devices.

FULL IBM SYSTEM/370 EMULATION

The AS/9000 processors are designed to be controlled by IBM System Control Programs (SCP's). The SCP's themselves contain large amounts of software used to recover from errors which might otherwise have caused the complete processor complex to 'shut-down'. Some of these 'software RAS' facilities require that the processor on which they are to be used is able to support 'machine dependant' instructions.

The AS/9000 is designed to support this SCP recovery software by providing emulation of certain specific 'DIAGNOSE' instruction formats. This means that unmodified IBM SCP's are able, for example, to delete part of the TLB or high speed buffer prior to retrying an instruction which caused a 'hard' failure in those parts of the hardware.

The ability of the AS/9000 to emulate some of the IBM machine dependent instructions allows the 9000 series processor to take advantage of the RAS facilities which are part of the IBM control programs.

DIAGNOSTIC FACILITIES

Should a malfunction occur then a number of different facilities are provided to ensure that a repair can be effected in the shortest possible time. The methods provided for the AS/9000 series are described in more detail below.

LOGOUT ANALYSIS (LOA)

A number of programs are provided within the Service Processor (SVP) which can be used to analyse the logout data which is automatically written to the SVP disk after the AS/9000 has detected a processor malfunction. The LOA programs are capable of pinpointing the individual package, or group of packages, which caused the failure recorded on the SVP disk storage. The LOA programs can also be run from the processor, but are normally run only from the SVP in parallel with normal user work.

The running of LOA programs in the SVP does not in any way effect the normal operations of the AS/9000 series, except that the SVP console display itself may be needed to control the LOA programs.

MICRODIAGNOSTICS (MD)

Microdiagnostics are a set of programs which run the processor complex in a stand-alone mode. These programs are written in microcode and are intended to locate faults in processor areas which are not covered by the Fault Locating Tests. The programs reside on a number of diskettes which are placed in the SVP and replace the diskette which normally holds the AS/9000 IBM System/370 microcode. The microdiagnostics are loaded into the AS/9000 control storage from the SVP maintenance frames.

The results of any fault diagnosis are displayed as an error code on the CRT screen of the SVP being used to run the tests.

FAULT LOCATING TEST (FLT)

A number of stand alone Fault Locating Programs (FLP's), written in internal

machine code, are provided. These programs are intended to locate any faults in the major parts of the BPU such as the IU and EU. The FLP's are held on both diskettes for operation from the SVP and on magnetic tape for loading from a peripheral device. An FLP is executed in a similar way to the microdiagnostics except that they can also be run from tape.

The testing of a processor using an FLP is called a Fault Locating Test (FLT).

TEST AND MAINTENANCE PROGRAMS

A number of programs, which run under the control of their own monitor, are provided for the AS/9000 of processors. These programs are used to carry out tests of the various functions of the processor hardware to ensure that they are working correctly. The programs also provide to the maintenance engineer the information needed to carry out a repair to a failing processor.

SVP MAINTENANCE FUNCTIONS

A number of special facilities are provided within the system which the engineer may use to assist him in resolving any problems which might occur in the processor complex. These facilities are used by means of special maintenance operator frames provided on the SVP Console Display. Full details of these frames is to be found in the engineering maintenance documentation. They will not normally be used by the user.

REMOTE SUPPORT

The SVP of the AS/9000 series has the capability of supporting a remote console via a normal telephone line. The SVP has all the necessary logic and control frames to monitor the use of the remote link. Once the teleprocessing link has been established then the remote console can carry out all the operator and control functions available from the normal SVP.

SPECIFICATIONS

AIR CONDITIONING

ENVIRONMENTAL SPECIFICATIONS

The air surrounding the product hardware must meet the specifications in table 6 below.

Condition	Temp. (°C)	Relative Humidity (%)	Wet Bulb Temp. (°C)
Operating	16-32	20-80	26
Non-operating	4-43	8-90	27
Recommended	21-24	55	-
Shipping	4-43	8-90	27

Table 6 - Environmental Air Requirements.

COOLING REQUIREMENTS

Under-the-floor cooling air must be provided. The air at the floor intakes to the AS/9000 series processor must have a positive pressure and meet the specifications given in table 7 below.

Condition	Value
Temperature §	10 to 20 (°C)
Relative Humidity	50 to 70 (%)
Altitude	0 to 3000 feet

§ For altitudes of from 3,000 to 7,000 feet above sea level, air temperature is decreased by 2°C for each 1,000 feet above 3,000 feet.

Table 7 - Cooling Air Requirements.

POWER REQUIREMENTS

- Input Voltage - 200V, 208V or 230V a.c.

  Machines shipped by National Advanced Systems (Europe) and its subsidiaries have a 'no-cost RPO' which in addition provides support for input voltages of 380 and 415 volts a.c.

- Input Cables - For the CPU and for main power of the CSVP a 3 phase, 3 wire, 4 conductor supply is required. For the auxiliary power of the CSVP and the convenience outlets a single phase, 2 wire, 3 conductor supply is required.

- Input Frequency - 50 Hz ±0.5 Hz (non UL approved) or 60 HZ ±0.5 HZ (UL approved).

- Voltage Limits - A transient voltage condition must not exceed plus 15% or minus 18% of nominal and must return to within a steady state tolerance of plus 10% or minus 8% of the normal rated voltage within 500 milliseconds.

POWER TOLERANCES

- Line-to-line imbalance voltage must not exceed 2.5%.

- Non-operating harmonic contents must not exceed 5%.

- 'Brown-out' of over 500 milliseconds will cause processor shutdown.

FLOOR PLANS

Figure 4 on page 21 shows the floor plan for the AS/9040, AS/9050 and the AS/9060. Figure 5 on page 22 shows the floor plan for the AS/9070 and the AS/9080 Figure 6 on page 23 shows the floor plan for the AS/9000 console and additional CTCA's.

These floor plans show the correct dimensions but are not drawn to scale.

Description	AS/9040	AS/9050	AS/9060	AS/9070	AS/9080
Basic Cycle Time (nanoseconds)	38	38	30	38	30
Cache Memory Size (Kilo/bytes)	32	64	256	2 * 64	2 * 256
Control Storage Size -					
BPU - 142 bit + 18 parity/word	16 Kword	16 Kword	16 Kword	16 Kword	16 Kword
IOP/ECG - 40 bit word §1	2 Kword	2 Kword	2 Kword	2 Kword	2 Kword
IOP/CHAN - 18 bit word §2	1 Kword	1 Kword	1 Kword	1 Kword	1 Kword
SVP - 9 bit word	128 KW	128 KW	128 KW	128 KW	128 KW
Translate Lookaside Buffer (TLB)	512	512	1024	2 * 512	2 * 1024
Segment Table Origin (STO)	128	128	128	2 * 128	2 * 128
HSA cycle time - nsecs.	19	19	15	19	15
Memory Interleave	8 way	8 way	8 way	16 way	16 way
Memory access (chip level) nsecs.	100	100	100	100	100
Memory reconfiguration size	2 Mbytes	2 Mbytes	2 Mbytes	4 Mbytes	4 Mbytes
Maximum Channel Data Transfer -					
Byte-multiplexor (Kbytes/sec)	100	100	100	100	100
Block-multiplexor (Mbytes/sec)	2	2	2	2	2
Data-streaming (Mbytes/sec)	3	3	3	3	3
Maximum Aggregate Data Rate -					
Per IOP (Mbytes per second)	20	20	>20	20	>20
Per BPU (Mbytes per second)	51	51	>60	42	>60
Per System (Mbytes per second)	51	51	>60	84	>100
Unit Control Words per channel	256	256	256	256	256

§1 ECG is Extended Channel Group.
§2 CHAN is each individual channel.

Figure 3 - AS/9000 Specification Comparison.

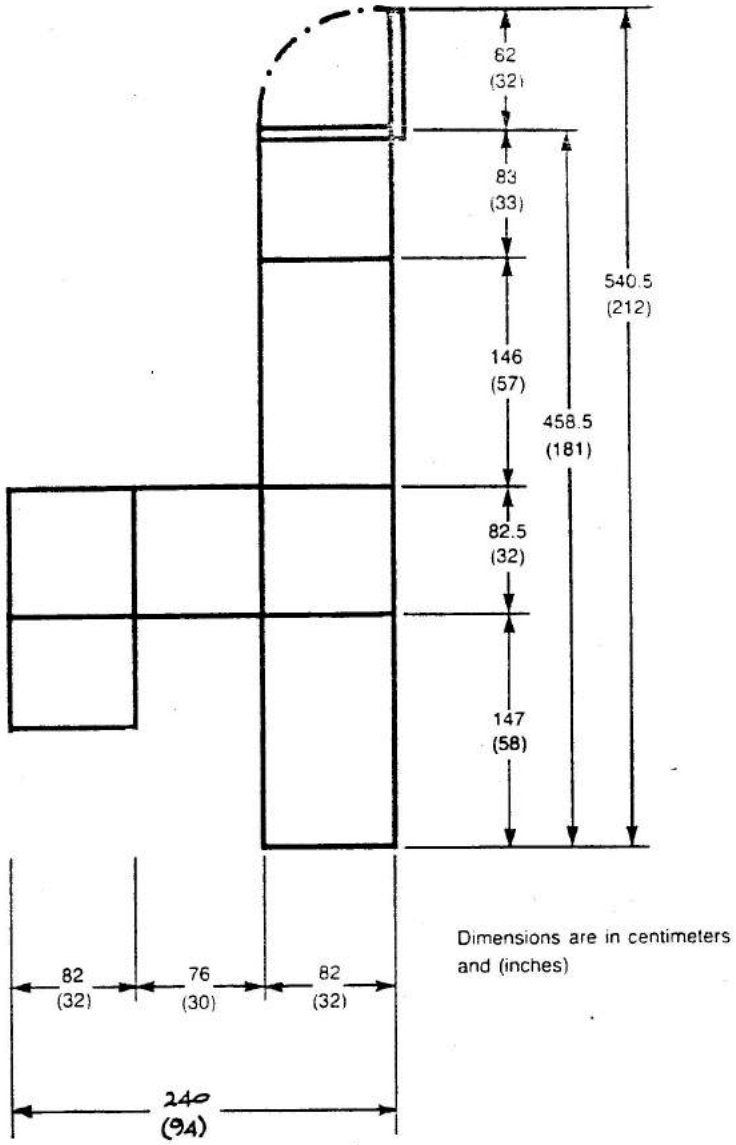

Figure 4 - AS/9040, AS/9050 and AS/9060 Floor Plan.

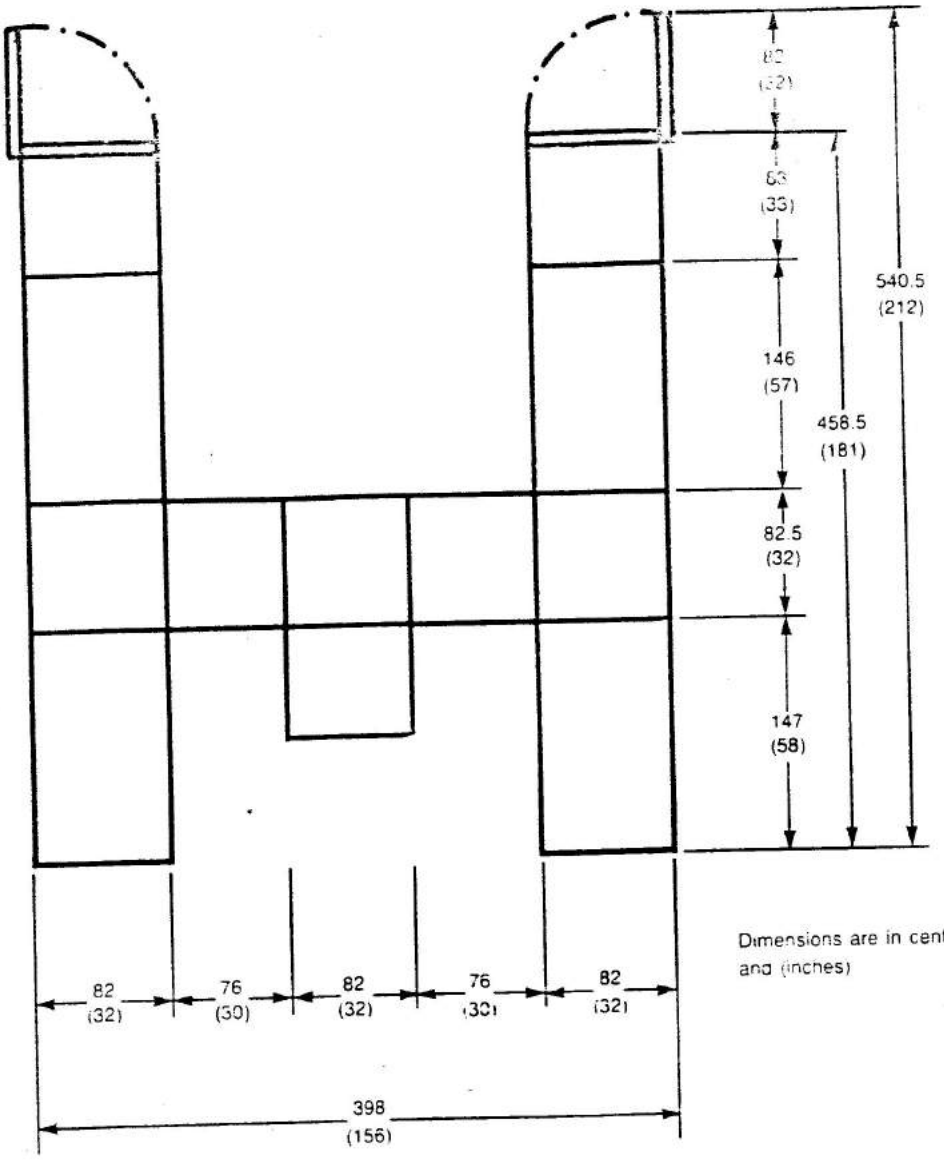

Figure 5 - AS/9070 and AS/9080 Floor Plan.

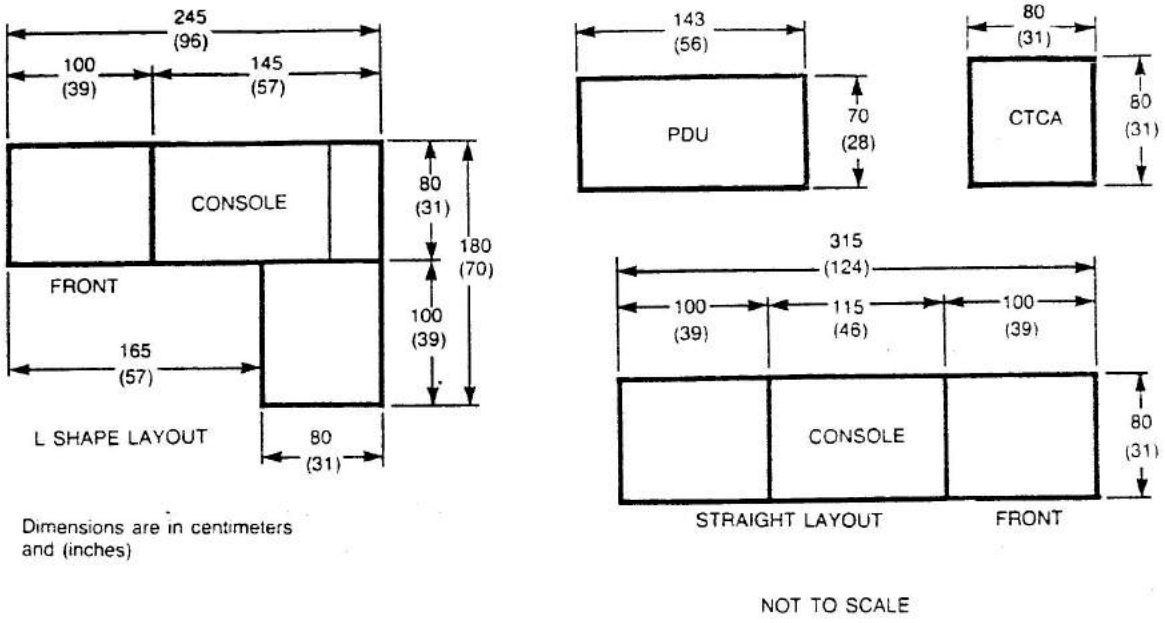

Figure 6 - AS/9000 Console/PDU/CTCA Floor Plans.

This page is for editorial purposes only.

APPENDIX A AS/9000 SPECIFICATION CHANGES

Introduction

During the life of the AS/9000 series of processors National Advanced Systems has made a number of improvements to the product specifications. These changes are the result of experience gained with the machines which have already been shipped and also as a part of the company's continued effort to bring to the market place the best and most reliable products possible.

This appendix describes the major changes to the specifications of the AS/9000 series.

Major Changes

There have been a number of major changes to the AS/9000 series product specifications and these are summarised below:-

- The basic model clock cycle time was changed from 40 to 38 nanoseconds.
- The original channels were replaced by the Extended Channel Groups.
- The original BPU logic has been updated to give improved performance and reliability to the AS/9000 series of processors.
- Memory has been enhanced by the use of 64K bit chips to replace the 16K bit chips used on the earlier models.

When these changes were implemented a number of other changes of a lesser nature were incorporated at the same time. The change descriptions below include information about these concurrent changes.

38 Nanosecond Clock

This particular change has two 'manifestations':-

- Within the NAS domestic marketplace (i.e. U.S.A., Canada, etc.) the AS/9000 basic model specifications were enhanced and a new model number, AS/9000-2, applied. The AS/9000-2 superceded the AS/9000 in the NAS domestic area.
- Within the NAS(Europe) marketplace the AS/9000 basic model specifications were enhanced but the new model number was not applied.

Since all of the original models shipped via NAS(Europe) have been upgraded to the new specification, then within Europe there is now no difference between the AS/9000 and the AS/9000-2 and the AS/9000-2 label is not used.

The change from 40 to 38 nanoseconds was made to improve the internal performance of the processor. The change could only be made after considerable testing had been done to verify that the reduction in clock cycle time did not in any way effect the reliability of the AS/9000.

At the same time that the cycle time of the clock was changed enhancements were made to the processor microcode to improve the performance of some instructions. This microcode change was transparent to the user since it did not change any 'function' of the processor.

Although the clock times of other models in the AS/9000 were not changed the microcode changes have been incorporated in all the other models in the range.

Extended Channel Groups

The Extended Channel Groups (ECG) and Extended Channel Adapters (ECA) were offered as a feature on the early AS/9000 models. They are now part of the standard specification for the AS/9000 series. This is a major change which basically gives a considerable enhancement to the capabilities of the AS/9000 series channels.

In the original processor configuration up to three Input Output Processors known as type 'C' (IOPC) could be attached to an IOPC adapter (IOPA'C') to provide up to 16 peripheral I/O channels per BPU. Each IOPC could have:-

- o A maximum of six channels in the first and second IOPC's.
- o A maximum of four channels in the third IOPC.
- o A maximum of two byte-multiplex channels per IOPC.
- o A maximum of two data-streaming channels per IOPC.
- o A lower maximum aggregate transfer rate than the ECG/ECA feature which replaced it.
- o A total of four physical frames to hold the 16 channels.

The IOPC of the original processors was replaced with the IOP Extended (IOPX) which gives considerable enhancements to the channel capabilities of the AS/9000 series processors. IOPX is known as the 'Extended Channel Group (ECG) feature'. The new IOPX with its enhanced facilities required that the IOPA be replaced to support them. The new IOPA'X' is known as the 'Extended Channel Adapter (ECA) feature'.

In order that all of the new capabilities of the ECG/ECA facility could be supported to the full it was necessary to increase the capacity of the Service Processor (SVP) control storage. The SVP storage size was thus extended from 96 K/words to 128 K/words.

With the ECG/ECA feature installed up to three ECG's can be attached to each ECA to give a total of up to 24 channels per ECA (IOPA'X'). Each ECG (IOPX) can have:-

- o Two four channel groups to give up to eight channels per ECG (IOPX).
- o A maximum of two byte-multiplex channels per ECG (IOPX).
- o All channels can be of any type. (Byte, block or data-streaming.)
- o A much higher aggregate data transfer rate than the old channels.

Since the ECG/ECA required that the SVP have more control storage a number of enhancements were made to the SVP which utilised some of this additional storage and have thus become part of the ECG/ECA feature. These include the following:-

- o Improvements to the layout of some of SVP control frames to make their use easier.
- o Changes to the configuration frames to provide for the new IOP's.
  - Allow any channel to be any type by entering the data from the SVP.
  - Allow any channel port to be assigned any logical number.
  - Enhance the reconfiguration possibilities.
- o Addition of a facility similar to that of the IBM System Status Recorder (SSR) to the SVP functions.

AS/9000 series processors which have the ECG/ECA feature installed no longer support the connection of peripheral devices using the 'Two-Byte Interface' feature. This feature was optionally available on AS/9000 series processors which made use of IOPC.

BPU Logic Enhancement

The AS/9060 and AS/9080 were introduced to the AS/9000 series of processors and made use of enhanced logic in the BPU. It was decided as part of the National Advanced Systems policy of bringing improved products to the customers to replace the original AS/9000 models with new ones based on the improved BPU. The new models, AS/9040, AS/9050 and AS/9070, therefore supersede the original AS/9000N, AS/9000 and AS/9000DPC models.

The new BPU has the following enhancements:-

- o Capable of operating with a reduced cycle time. (Down to 30 nanoseconds.)
- o An improved I Unit logic which reduces the time for some instructions which use long operands from storage.
- o More use is made of VLSI to improve performance, increase reliability and reduce the power requirements.
- o Designed to reduce the data storage contention from the levels of the earlier models.

Although the new models are designed to supersede the earlier ones with performance levels which are comparable this can't be completely done due to the changes in the BPU which will enhance the performance of some specific instructions more than others. In general performance of the new models

will be similar to that of the original models except where there is a predominance of the storage to storage type of instructions when the new models may be faster than the old ones.

Memory Enhancement

The use of 16k bit memory chips has been superseded by the use of chips containing 64k bits. This increase in the density of storage components, 1 Megabyte of storage now requires only one package, permits the maximum storage available to be increased whilst at the same time reducing the power requirements of the new models.

On the new models up to 32 M/bytes can contained in one memory frame. The earlier models required a second memory frame as soon as the storage exceeded 16 M/bytes, and the maximum storage size was 32 M/bytes contained in two storage frames.


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